Bypass Design Problem

As was mentioned in class, one design philosophy for wide-band noise filtering is to use two parallel capacitors, one with large capacitance (and corresponding large parasitic ESL) to filter low frequencies, and one with smaller capacitance (and corresponding lower parasitic ESL) to filter higher frequencies. In addition, it is often desired for the net impedance of the combination to be relatively constant over the intended bandwidth. One way to accomplish this is to design these capacitors so that they have the same asymptotic impedance (from their Bode diagrams, see Figure 5.17 of the text) at their respective resonant frequencies.

What is easy to neglect in this idea is that the parallel combination of these components will have an antiresonance somewhere between the parallel resonant frequencies that can seriously impact the effectiveness of this technique. The solution to this problem is to make sure that both capacitors have sufficient series resistance (ESR) to damp out this antiresonance. To demonstrate, design a parallel capacitor combination that has no more than 3dB of impedance ripple at frequencies between the two resonant frequencies.

C1 – 22 uF , with 1.15 nH of ESL, and arbitrary ESR

C2 is unknown, but should resonate at 10 MHz and have the same asymptotic impedance at its resonant frequency as C1 does at its resonant frequency

Specify all the parameters of C2 (C, ESL, ESR) and the required ESR of C1 that maintains no more than 3dB impedance ripple between 1 and 10 MHz. Also, specify the quality (Q) factors of both capacitors. Show a Bode plot of the combined impedance over the frequency range 0.1 MHz to 100 MHz, and also show the impedance of same network with no ESR values for either capacitor. Comment on the difference in these responses and the design tradeoffs.